AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in this application:

LISTING OF THE CLAIMS:

1-24. (Canceled).

25. (Currently Amended) A method for processing operands in a processing unit having at least two execution units, comprising:

operating the ~~executing~~ execution units at a predefinable clock cycle;

triggering the execution units by control signals for a processing of the operands;

switching between a first operating mode and a second operating mode;

in the first operating mode, supplying the execution units with the same operands; ~~and~~

in the second operating mode, supplying the execution units with different operands, wherein:

the execution units are triggered by the same control signals for the processing of the operands in the first operating mode, and

the execution units are controlled by different control signals for the processing of the operands in the second operating mode; and

in the first operating mode, comparing the operands and resulting data through a comparator to check for agreement, wherein the operands and the resulting data are released and written to a bus if in agreement, and wherein the operands and the resulting data are withheld and written to an error register if not in agreement.

26. (Currently Amended) The method as recited in claim 25, further comprising:

in the first operating mode, supplying the operands to the execution units as a function of the clock cycle for operand processing of the execution units in the form of a full cycle; and

in the second operating mode, supplying the operands at a second clock cycle for the processing of the operands, the second cycle being faster than the full cycle, one of the execution units thereby receiving operands after a time offset passes from a time at which another of the execution units receives operands in a same clock cycle.

27. (Previously Presented) The method as recited in claim 26, wherein in the first operating mode the operands are supplied at the clock cycle of the execution units, as full cycle.

28. (Previously Presented) The method as recited in claim 26, wherein, compared to the full cycle, the faster second clock cycle is designed as half cycle and is twice as fast and the time offset is equal to half of the full cycle.

29. (Previously Presented) The method as recited in claim 25, wherein the execution units process the operands in synchrony in the first operating mode and the second operating mode.

30. (Previously Presented) The method as recited in claim 25, further comprising:

processing the operands in synchrony in the first operating mode; and

processing the operands in asynchrony in the second operating mode.

31. (Currently Amended) The method as recited in claim 25, further comprising:

~~comparing one of the operands and data derived from the operands for agreement; and~~

detecting an error in case of a deviation.

32. (Currently Amended) The method as recited in claim 25, further comprising:

comparing one of states and results produced in the processing of the operands for agreement; and

detecting an error in a deviation, the comparison being implementable as a function of [[the]] <u>an</u> individual operating mode.

33. (Previously Presented) The method as recited in claim 32, further comprising:

releasing the one of the states and the results by a release signal as a function of the operating mode and the comparison.

34. (Currently Amended) The method as recited in claim 32, further comprising:

releasing the one of the states and <u>the</u> results ~~by a release signal one of~~ simultaneously ~~and successively~~ as a function of the operating mode.

35. (Currently Amended) A device for operand processing in a processing unit having at least two execution units, comprising:

an arrangement for operating the execution units at a predefinable clock cycle; and

a control unit for triggering the execution units by control signals for a processing of [[the]] operands and for switching between a first operating mode and a second operating mode, wherein:

the control unit is connected to the execution units and additional feed units,

the control unit cooperates with the feed units so ~~in such a way~~ that ~~both~~ the at least two execution units are supplied with the same operands in the first operating mode and ~~both~~ the at least two execution units are supplied with different operands in the second operating mode, and

the control unit is configured so ~~being designed such~~ that ~~both~~ the at least two execution units are triggered by identical control signals for the processing of the operands in the first operating mode and ~~both~~ the at least two execution units are triggered by different control signals for the processing of the operands in the second operating mode; and

a comparator for checking, in the first operating mode, for agreement between the operands and resulting data, wherein the operands and the resulting data are released and written to a bus if in agreement, and wherein the operands and the resulting data are withheld and written to an error register if not in agreement.

36. (Currently Amended) The device as recited in claim 35, wherein the control unit and the feed units are configured so ~~designed such~~ that in the first operating mode the operands are supplied to the execution units as a function of the clock cycle of the execution units, as full cycle, and in the second operating mode the operands are supplied for processing at a second clock cycle, which is faster than the full cycle, one of the execution units thereby receiving operands after a time offset passes from a time at which another of the execution units receives operands in a same clock cycle.

37. (Previously Presented) The device as recited in claim 35, wherein the execution units are embodied as at least one of arithmetic logic units, floating point units, processors, and a

coprocessor.

38. (Previously Presented) The device as recited in claim 35, wherein the feed units and the execution units are designed such that in the first operating mode they operate in synchrony using an identical clock cycle.

39. (Currently Amended) The device as recited in claim 35, wherein the feed units [[as]] is a register system [[are]] that is configured so ~~designed such~~ that at least one operand register is provided and at least one buffer register is provided between the at least one operand register and each execution unit.

40. (Previously Presented) The device as recited in claim 35, wherein the feed units and the execution units are designed such that they operate at different clock cycles in the second operating mode.

41. (Previously Presented) The device as recited in claim 35, wherein the feed units are designed such that in the second operating mode they operate at a clock cycle that is twice as fast as that of the execution units.

42. (Previously Presented) The device as recited in claim 35, further comprising:

a decoder by which a switchover condition is detectable, wherein the decoder operates at the same clock cycle as the feed units.

43. (Currently Amended) The device as recited in claim 35, further comprising:

a comparison arrangement designed such that ~~one of~~ the operands and data derived from the operands are compared for agreement, wherein an error is detected in case of a deviation.

44. (Currently Amended) The device as recited in claim 35, ~~further comprising: a comparison arrangement~~ wherein the comparator further compares ~~designed such that~~ states produced in the processing of the operands ~~are compared~~ for agreement, and wherein an error is detected in case of a deviation.

45. (Previously Presented) The device as recited in claim 35, further comprising:

a first switching arrangement for switching the operands from the feed units as a function of one of the first operating mode and the second operating mode.

46. (Previously Presented) The device as recited in claim 45, further comprising:

a second switching arrangement for activating the execution units as a function of one of the first operating mode and the second operating mode.

47. (Currently Amended) A processing unit, comprising:

a device for operand processing having at least two execution units that are able to be operated at a predefinable clock cycle; and

a control unit for ~~triggers~~ triggering the execution units by control signals for the processing of [[the]] operands and for switching between a first operating mode and a second operating mode, wherein:

the control unit is connected to the execution units and additional feed units,

the control unit cooperates with the feed units in such a way that ~~both~~ the at least two execution units are supplied with the same operands in the first operating mode and ~~both~~ the at least two execution units are supplied with different operands in the second operating mode, and

the control unit is configured so ~~being designed such~~ that in the first operating mode ~~both~~ the at least two execution units are triggered by the same control signals for the processing of the operands and in the second operating mode ~~both~~ the at least two execution units are triggered by different control signals for the processing of the operands; and

a comparator for checking, in the first operating mode, for agreement between the operands and resulting data, wherein the operands and the resulting data are released and written to a bus if in agreement, and wherein the operands and the resulting data are withheld and written to an error register if not in agreement .

48. (New) The method as recited in claim 32, further comprising:

releasing the one of the states and the results successively as a function of the operating mode.

49. (New) A method for processing operands in a processing unit having at least two execution units, comprising:

operating the execution units at a predefinable clock cycle;

triggering the execution units by control signals for a processing of the operands;

switching between a first operating mode and a second operating mode;

in the first operating mode, supplying the execution units with the same operands; ~~and~~

in the second operating mode, supplying the execution units with different operands, wherein:

the execution units are triggered by the same control signals for the processing of the operands in the first operating mode, and

the execution units are controlled by different control signals for the processing of the operands in the second operating mode;

in the first operating mode, supplying the operands to the execution units as a function of the clock cycle for operand processing of the execution units in the form of a full cycle; and

in the second operating mode, supplying the operands at a second clock cycle for the processing of the operands, the second cycle being faster than the full cycle, one of the execution units thereby receiving operands after a time offset passes from a time at which another of the execution units receives operands in a same clock cycle.

50. (New) The method as recited in claim 49, wherein in the first operating mode the operands are supplied at the clock cycle of the execution units, as full cycle.

51. (New) The method as recited in claim 49, wherein, compared to the full cycle, the faster second clock cycle is designed as half cycle and is twice as fast and the time offset is equal to half of the full cycle.

52. (New) A device for operand processing in a processing unit having at least two execution units, comprising:

an arrangement for operating the execution units at a predefinable clock cycle; and

a control unit for triggering the execution units by control signals for a processing of operands and for switching between a first operating mode and a second operating mode, wherein:

the control unit is connected to the execution units and additional feed units,

the control unit cooperates with the feed units so that the at least two execution units are supplied with the same operands in the first operating mode and the at least two execution units are supplied with different operands in the second operating mode, and

the control unit is configured so that the at least two execution units are triggered by identical control signals for the processing of the operands in the first operating mode and the at least two execution units are triggered by different control signals for the processing of the operands in the second operating mode;.

wherein the control unit and the feed units are configured so that in the first operating mode the operands are supplied to the execution units as a function of the clock cycle of the execution units, as full cycle, and in the second operating mode the operands are supplied for processing at a second clock cycle, which is faster than the full cycle, one of the execution units thereby receiving operands after a time offset passes from a time at which another of the execution units receives operands in a same clock cycle.